REMARKS

The Examiner's Office Action of July 30, 2003 has been received and its contents reviewed. Applicant would like to thank the Examiner for the consideration given to the above-identified application.

Claims 1-6 and 15-28 are pending for consideration, of which claims 1, 3, 5, 15, 20, 23, 25 and 27 are independent. By the above actions, claims 1, 3, and 5 have been amended. In view of these actions and the following remarks, reconsideration of this application is now requested.

Referring now to the detailed Office Action, claims 1-6 stand rejected under 35 U.S.C. §102(b) as anticipated by Asai et al. (U.S. Patent No. 5,365,875 – hereafter Asai). Further, claims 15, 16, 19, 20, 22, 25 and 26 stand rejected under 35 U.S.C. §103(a) as unpatentable over Applicant's prior art as shown in Figure 5, in view of Asai. Finally, claims 17, 18, 21, 23, 24, 27 and 28 stand rejected under 35 U.S.C. §103(a) as unpatentable over Applicant's prior art in view of Asai and further in view of Dabral et al. (U.S. Patent No. 6,090,650 – hereafter Dabral).

With respect to the §102(b) rejection over Asai, in response to the Examiner reasoning that the transistor used in a buffer circuit in the original claims 1-6 are considered an intended use and do not serve to further the structure of the claims, Applicant has amended independent claims 1, 3, and 5, as shown above, to further clarify the claim language. Specifically, claims 1, 3, and 5 have been amended to recite the analog buffer as comprising at least one of a current mirror circuit, a differential circuit, and the one of the current mirror circuit and the differential circuit comprising at least a first and second thin film transistor. As amended, claims 1, 3, and 5 clearly does not recite the analog buffer merely as intended use but as a structure.

Applicant respectfully assert that the Asai reference does not disclose a buffer. More specifically, Asai does not disclose a buffer comprising at least one of a current mirror circuit, a differential circuit, and the one of the current mirror circuit and the differential circuit comprising at least a first and second thin film transistor. Instead, Arai appears to be directed to the method of manufacturing thin film transistor for general use in liquid crystal panels or a contact type image sensor (see col. 3, lines 29-31).

Anticipation requires the presence in a single prior art reference disclosure of each

and every element of the claimed invention, arranged as in the claim. Lindemann Maschinenfabirk Gmbh v. American Hoist & Derrick, 221 USPQ 481, 485 (Fed. Cir. 1984). Asai clearly fails to disclose structure positively recited and claimed in claims 1, 3, and 5. Specifically, Asai fails to disclose a buffer comprising at least one of a current mirror circuit, a differential circuit, and the one of the current mirror circuit and the differential circuit comprising at least a first and second thin film transistor. Therefore, the §102(b) rejection is improper and respectfully requested to be reconsidered and withdrawn.

With respect to the §103(a) rejections which are based on Asai as the primary reference, Applicant respectfully submit that the arguments set forth above with respect to the §102(b) rejection are also applicable to the §103(a) rejections. Further, as discussed above, Asai appears to teach that the semiconductor layer is made uniform in crystallinity due to an excimer laser irradiation with a desirable energy, not controlling gate width and length. Therefore, Asai does not provide the required motivation or suggestion to combine its teaching with that of Applicant's admitted prior art or Dabral.

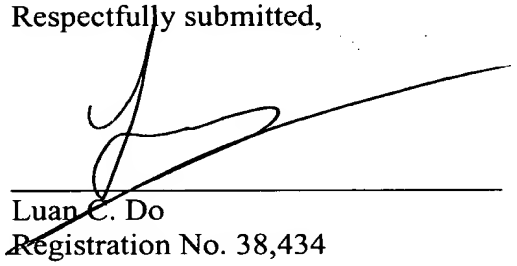
In other words, Asai's attempt to ensure that the semiconductor layer is uniform with regard to crystallinity by controlling the energy level of a laser does not motivate one of ordinary skill to modify Asai to include an analog buffer and such features as the differential circuit, current mirror circuit, and the current source recited in amended independent claims 15, 20, 23, 25, and 27.

The requirements for establishing a *prima facie* case of obviousness, as detailed in MPEP § 2143 - 2143.03 (pages 2100-122 - 2100-136), are: first, there must be some suggestion or motivation, either in the reference themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference to combine the teachings; second, there must be a reasonable expectation of success; and, finally, the prior art reference (or references when combined) must teach or suggest all of the claim limitations. As Asai is deficient in an analog buffer comprising at least one of a current mirror circuit, a differential circuit, and the one of the current mirror circuit and the differential circuit comprising at least a first and second thin film transistor, its combination with Applicant's prior art or Dabral, especially without proper motivation or suggestion, would be improper.

In view of the amendments and arguments set forth above, Applicant respectfully requests reconsideration and withdrawal of all the pending rejections.

While the present application is now believed to be in condition for allowance, should the Examiner find some issue to remain unresolved, or should any new issues arise, which could be eliminated through discussions with Applicant's representative, then the Examiner is invited to contact the undersigned by telephone in order that the further prosecution of this application can thereby by expedited.

Respectfully submitted,



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